IN THE CLAIMS

The pending claims are reproduced below.

1-39. (Canceled)

40. (Previously Presented) A substrate comprising:

a first dielectric layer;

a second dielectric layer;

a first conductive layer between the first and second dielectric layers;

a third dielectric layer, the second dielectric layer being between the first and third dielectric layers;

a second conductive layer between the second dielectric layer and the third dielectric layer, the second conductive layer including a first skip via that extends through the first and second dielectric layers; and

a third conductive layer on the third dielectric layer, the third conductive layer including a second via that extends through the third dielectric layer, the second via and the first skip via being stacked on top of one another.

41. (Previously Presented) The substrate of claim 40 wherein the first skip via includes a longitudinal axis and the second via includes a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second via.

42. (Previously Presented) The substrate of claim 41 wherein the first, second and third dielectric layers are formed on a core.

43. (Previously Presented) The substrate of claim 42 further comprising a fourth conductive layer between the first dielectric layer and the core.

44. (Previously Presented) The substrate of claim 40 wherein the first, second and third conductive layers are patterned conductive layers.

45. (Previously Presented) The substrate of claim 40 wherein the first skip via has a diameter between 49um and 85um and the second via has a diameter between 49um and 85um.

46. (Previously Presented) The substrate of claim 40 wherein the first skip via has a length between 58um and 92um and the second via has a length between 24um and 36um.

47. (Previously Presented) A substrate comprising:

a first dielectric layer;

a second dielectric layer;

a first conductive layer between the first and second dielectric layers;

a third dielectric layer, the second dielectric layer being between the first and third dielectric layers;

a second conductive layer between the second and third dielectric layers, the second conductive layer including a first skip via that extends through the first and second dielectric layers;

a fourth dielectric layer, the third dielectric layer being between the second and fourth dielectric layers;

a third conductive layer between the third and fourth dielectric layers; and

a fourth conductive layer on the fourth dielectric layer, the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers, the second skip via and the first skip via being stacked on top of one another.

48. (Previously Presented) The substrate of claim 47 wherein the first skip via and the second skip via each include a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second skip via.

49. (Previously Presented) The substrate of claim 47 wherein the first, second, third and fourth dielectric layers are formed on a core.

50. (Previously Presented) The substrate of claim 49 further comprising a fifth conductive layer between the first dielectric layer and the core.

51. (Previously Presented) The substrate of claim 47 wherein the first, second, third and fourth conductive layers are patterned conductive layers.

52. (Previously Presented) The substrate of claim 47 wherein the first skip via has a diameter between 49um and 85um and the second skip via has a diameter between 49um and 85um.

53. (Previously Presented) The substrate of claim 47 wherein the first skip via has a length between 58um and 92um and the second skip via has a length between 58um and 92um.

54. (Previously Presented) The substrate of claim 47 further comprising:

a fifth dielectric layer, the fourth conductive layer being between the fourth and fifth dielectric layers;

a sixth dielectric layer, the fifth dielectric layer being between the fourth and sixth dielectric layers;

a fifth conductive layer between the fifth and sixth dielectric layers;

a sixth conductive layer on the sixth dielectric layer, the sixth conductive layer including a third skip via that extends through the fifth and sixth dielectric layers.

55. (Previously Presented) The substrate of claim 54 wherein the first, second and third skip vias each include a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second and third skip vias.

56. (Previously Presented) The substrate of claim 54 wherein the first, second, third, fourth, fifth and sixth conductive layers are patterned conductive layers.

57. (Previously Presented) The substrate of claim 54 wherein the first, second and third skip via each have a diameter between 49um and 85um.

58. (Previously Presented) The substrate of claim 54 wherein the first, second and third skip via each have a length between 58um and 92um.